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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

WILLIAM P. STEARNS ET AL.

Serial No. 09/678.318 (TI-25833.1)

Filed October 3, 2000

For: OPTIMIZED CIRCUIT DESIGN LAYOUT FOR HIGH PERFORMANCE BALL GRID ARRAY PACKAGES

Art Unit 2815

Examiner P. Brock, II

Commissioner for Patents
Washington, D. C. 20231

Sir:

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of the final rejection of claims 1 to 8 and 20 to 27, all of the rejected claims. Claims 19 and 28 have been objected to and considered to be allowable.

Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was not filed after the final rejection.

SUMMARY OF INVENTION

The invention relates to a method of laying out traces (9) for connection of bond pads (8) of a semiconductor chip (5) to a ball grid array (13) disposed on a substrate (1). The steps include providing a substrate (1)having a surface with a plurality of rows and columns of ball pads (15) and having a solder ball (13) secured to each of the ball pads. As best shown in Figs. 3 and 4, a plurality of pairs of traces are provided on the surface, each trace of each of the pairs of traces extending to a different one of the ball pads and extending to ball pads on a plurality of the rows and columns, each trace of each of the pairs of traces being spaced from the other trace of the pair by up to a ball pitch, being maximized for identity in length, having up to one ball pitch difference in length and being maximized for parallelism and spacing. Each of the traces of the pair is preferably further maximized for identity in cross-sectional geometry. A differential signal pair is preferably applied to at least one of pair of traces. A further surface insulated from the prior mentioned surface is preferably provided with a plurality of the traces being disposed on the further surface. As shown in Fig. 4, the substrate preferably has at least first, second and third rows and first, second, third and fourth columns of the ball pads in a matrix array, a first trace of a first pair of the traces extending to a ball pad in the first row of the second column closest to the chip and a second trace of the first pair of traces extending to a ball pad in the second row of the second column and between the first column and second column which is adjacent to the first column, a first trace of a second pair of the traces extending to a ball pad in the first row of the third column closest to the chip and a second trace of the second pair of traces

extending to a ball pad in the second row of the third column and between the third column and the fourth column which is adjacent to the third column, and first and second traces of a third pair of the traces extending to ball pads in the third row of the second and third columns and disposed between the second and third columns. The substrate is preferably a printed wiring board substrate.

ISSUES

The issues on appeal are as follows:

1. Whether claims 1, 2, 20 and 21 are anticipated by Ohsawa (U.S.2000/001449 A1) under 35 U.S.C. 102(a)

2. Whether claims 3, 4, 22 and 23 are patentable over Ohsawa under 35 U.S.C. 103(a).

3. Whether claims 5 to 8 and 24 to 27 are patentable over Ohsawa in view of Karnezos (U.S. 5,409,865) under 35 U.S.C. 103(a).

GROUPING OF CLAIMS

The claims do not stand or fall together for reasons set forth hereinbelow under ARGUMENT.

ARGUMENT

ISSUE 1

Claims 1, 2, 20 and 21 were rejected under 35 U.S.C. 102(a) as being anticipated by Ohsawa (U.S. 2001/001491 A1). The rejection is without merit.

Claim 1 requires, among other features, the step of providing a plurality of pairs of traces on the surface, each trace of each of the pairs of traces extending to a different one of

the ball pads and extending to ball pads on a plurality of the rows and columns, each trace of each of the pair of traces being spaced from the other trace of the pair by up to a ball pitch, being maximized for identity in length and having up to one ball pitch difference in length and being maximized for parallelism and spacing. No such step is taught or even remotely suggested by Ohsawa either alone or in the combination as claimed..

The final rejection states that the above step is shown in Fig. 3j of Ohsawa. However, a reading of the specification of Ohsawa and of that figure nowhere teaches or even remotely suggests the claimed step, regardless of the examiner's allegations to the contrary. It is further noted that the Examiner specifically stated in the reasons for allowance in the parent application that "Lee et al. fail to teach each trace of each pair [of] traces being spaced apart from the other trace of the pair by up to a ball pitch, being maximized for identity in length and having up to one ball pitch difference in length and being maximized for parallelism and spacing". This is precisely the language used in claim 1. It is repeated that this step is nowhere taught or even remotely suggested by Ohsawa.

Claims 2, 20 and 21 depend from claim 1 and therefore define patentably over Ohsawa for at least the reasons set forth above with reference to claim 1.

Claim 2 further limits claim 1 by requiring that each of the traces of the pair be further maximized for identity in cross-sectional geometry. No such feature is taught or suggested by Ohsawa either alone or in the combination as claimed.

Claims 20 and 21 further limit claims 1 and 2 by requiring that the substrate be a printed wiring board substrate. No such combination is taught or suggested by Ohsawa.

ISSUE 2

Claims 3, 4, 22 and 23 were rejected as being unpatentable over Ohsawa under 35 U.S.C. 103(a). The rejection is without merit.

Claims 3, 4, 22 and 23 depend from claim 1 and therefore define patentably over Ohsawa for at least the reasons set forth above as to claim 1.

In addition, claims 3 and 4 further limit claims 1 and 2 by requiring the step of applying a differential signal pair to at least one of a pair of the traces. No such combination is taught or suggested by Ohsawa.

Claims 22 and 23 further limit claims 3 and 4 by requiring that the substrate be a printed wiring board substrate. No such combination is taught or suggested by Ohsawa.

ISSUE 3

Claims 5 to 8 and 24 to 27 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ohsawa in view of Karnezos (U.S. 5,409,865). The rejection is without merit.

Claims 5 to 8 and 24 to 27 depend from claim 1 and therefore define patentably over Ohsawa in view of Karnezos for at least the reasons set forth above with reference to claim 1 since Karnezos fails to overcome the deficiencies in Ohsawa as noted above.

In addition, claims 5 to 8 further limit claims 1 to 4 by requiring the step of providing a further surface insulated from the surface, a plurality of the traces being disposed on the further surface. No such combination is taught or suggested by Ohsawa, Karnezos or any proper combination of these references.

Claims 24 to 27 further limit claims 5 to 8 by requiring that the substrate be a printed wiring board substrate. No such combination is taught or suggested by Ohsawa, Kamezos or any proper combination of these references.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

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APPENDIX

The claims on appeal read as follows:

1. A method of laying out traces for connection of bond pads of a semiconductor chip to a ball grid array disposed on a substrate, which comprises the steps of:

(a) providing a substrate having a surface with a plurality of rows and columns of ball pads and having a solder ball secured to each of said ball pads; and

(b) providing a plurality of pairs of traces on said surface, each trace of each of said pairs of traces extending to a different one of said ball pads and extending to ball pads on a plurality of said rows and columns, each trace of each of said pair of traces being spaced from the other trace of said pair by up to a ball pitch, being maximized for identity in length and having up to one ball pitch difference in length and being maximized for parallelism and spacing.

2. The method of claim 1 wherein each of said traces of said pair is further maximized for identity in cross-sectional geometry.

3. The method of claim 1 further comprising the step of applying a differential signal pair to at least one of a said pair of traces.

4. The method of claim 2 further comprising the step of applying a differential signal pair to at least one of a said pair of traces.

5. The method of claim 1 further including the step of providing a further surface insulated from said surface, a plurality of said traces being disposed on said further surface.

6. The method of claim 2 further including the step of providing a further surface insulated from said surface, a plurality of said traces being disposed on said further surface.

7. The method of claim 3 further including the step of providing a further surface insulated from said surfaces, a plurality of said traces being disposed on said further surface.

8. The method of claim 4 further including the step of providing a further surface insulated from said surface, a plurality of said traces being disposed on said further surface.

19. The method of claim 1 wherein said substrate has at least first, second and third rows and first, second, third and fourth columns of said ball pads in a matrix array, a first trace of a first pair of said traces extending to a ball pad in said first row of said second column closest to said chip and a second trace of said first pair of traces extending to a ball pad in said second row of said second column and between said first column and second column which is adjacent to said first column, a first trace of a second pair of said traces extending to a ball pad in said first row of said third column closest to said chip and a second trace of said second pair of traces extending to a ball pad in said second row of said third column and between said third column and said fourth column which is adjacent to said third column, and first and second traces of a third pair of said traces extending to ball pads in said third row of said second and third columns and disposed between said second and third columns.

20. The method of claim 1 wherein said substrate is a printed wiring board substrate.

21. The method of claim 2 wherein said substrate is a printed wiring board substrate.

22. The method of claim 3 wherein said substrate is a printed wiring board substrate.

23. The method of claim 4 wherein said substrate is a printed wiring board substrate.

24. The method of claim 5 wherein said substrate is a printed wiring board substrate.

25. The method of claim 6 wherein said substrate is a printed wiring board substrate.

26. The method of claim 7 wherein said substrate is a printed wiring board substrate.

27. The method of claim 8 wherein said substrate is a printed wiring board substrate.

28. The method of claim 19 wherein said substrate is a printed wiring board